國 立 清 華 大 學

碩 士 論 文

題目：考慮即時性測試下單元位置之 X 分佈以增加 X 填值減輕壓降效應的影響

A Physical-Location-Aware IR-Drop and Peak Current Reduction Using Fault Redistribution

系 所 別： 資訊工程學系碩士班

學號姓名： 9662586 林詠勝 (Yung-Sheng Lin)

指導教授： 黃婷婷 博士 (TingTing Hwang)

中華民國九十八年七月

中文摘要

隨著製程的進步、單位元件尺寸的縮小，邏輯閘延遲的缺陷更顯嚴重。為了確保電路上的時序要求，即時性測試被廣泛應用在測試電路的效能。然而，在即時性測試的當下，可能導致數量可觀的元件同時發生轉換，使得晶片內部的供電不穩定，產生所謂的電流電阻壓降效應。這會電路功能發生錯誤，並誤判電路本身為錯誤。故我們需要設法降低在即時性測試中的元件轉換率。

X 填值的方法最常被人用來解決即時性測試的電流電阻壓降效應，X 值的比例和特性則支配 X 填值的方法的效能。然而目前為止，還未有一個專門針對特定區域增加 X 值的演算法，以達到減低單位區塊內元件同時發生的轉換。

在這篇論文中，我們改變以往晶片測試中，增加測試樣本 X 分佈的方法 – 平均分佈或最大 X 數量，我們提出一個針對特定壓降區域增加 X 值的方法；加入考慮電路裡各元件的實際位置後，我們針對實際影響該區域的測試位元作測試舒緩，達到減少測試時發生的大量元件轉換，進而解決測試時產生的壓降效應。

A Physical-Location-Aware IR-Drop and Peak Current Reduction Using Fault Redistribution

Student: Yung-Sheng Lin
Advisor: TingTing Hwang

Department of Computer Science
National Tsing Hua University
HsinChu, Taiwan 300

Contents

List of Figures

List of Tables

Abstract

To guarantee an application specific integrated circuits (ASIC) meets the timing requirement, at-speed scan testing becomes an indispensable procedure to verify the performance of ASIC. However, at-speed scan test suffers from the test-induced yield loss. Because, the switching activity in testing is often higher than that in normal function. The switching-induced large current withdrawing in turn causes severe IR drop and increases gate delay. *X-filling* is the most commonly used technique to reduce IR-drop effect during at-speed test. Nevertheless, none of the existing test relaxation schemes taking the physical location of *X*-bits into account. Hence it is adversely affecting the effectiveness of reducing switching activities of IR-drop hot zone. In this thesis, we propose a novel test relaxation approach - Physical-Location-Aware X-Identification, which consider the physical information of sensitized scan cells induced switching activities. The experiment results on ITC'99 shows that we have average 42.70% potential transition reduction for the IR-drop hot zone.

Chapter 1

Introduction

As the fabrication process advances, the feature size scales down. The uncertainty of a gate delay increases significantly, and the IR-drop effect caused by high power density also impacts the timing severely. To guarantee an application specific integrated circuits (ASIC) meets the timing requirement, a delay fault testing becomes an indispensable procedure to verify the performance the ASIC.

The at-speed testing has been widely used for delay fault testing due to its easy implementation and efficient fault diagnosis [1]. For example, [2] reports that the defect per million rates are reduced by 30 to 70 percent when at-speed testings are integrated to the traditional stuck-at tests. In addition, it shows that the escape rate increases by almost 3 percent if the at-speed scan test is removed from the test program in a 0.13-micron fabrication process.

In at-speed testing, scan test is the most commonly used technique [3]. Nevertheless, scan test suffers from power and *IR-drop* issues. Shift power and capture power during scan test could be much higher than the power in normal operation [4, 5]. Thus, power consumption related issues in the shift mode and capture mode must be taken into account when it comes

to at-speed testing.

Since it takes most of the time to shift-in/shift-out test vectors to scan chains, the shift mode dominates the whole energy consumption of the testing process, and the accumulated effect of test power dissipation of circuit under test (CUT). Although the capture mode has limited effect on CUT's accumulated energy consumption, it causes a lot of gate switchings within a very short period and causes peak current consumption. The large current withdrawn in turn causes severe IR drop and increases gate delay. Moreover, test vector generators compress patterns as many as possible to reduce test cube. Thus, the switching activity in testing is often higher than in normal function, and lead to IR-drop.

Post-ATPG X-filling is one of the approaches to reduce switching activity by filling unspecified bits in test patterns. In general, there are over 50% X-bits in most of test cubes. X-filling approach is to keep circuit from transition except target faults by filling X-bits in test vectors. However the performance of post-ATPG X-filling is determined by the number and characteristic of X-bits. The more X-bits in a test cube the bigger solution space of the X-filling is. In addition, if the X-bits are associated to the switchings of IR-drop regions, we can reduce the IR-drop by filling appropriate values to these X-bits. Many researches [6, 8] have been proposed to perform X-filling.

Yet, there is one more important issue to be discussed - fault distribution. First, many faults in a single test vector may lower the *X*-bits rate and reduce the effectiveness of *X*-filling. Second, the propagation path of target faults is also an important concern. For example,

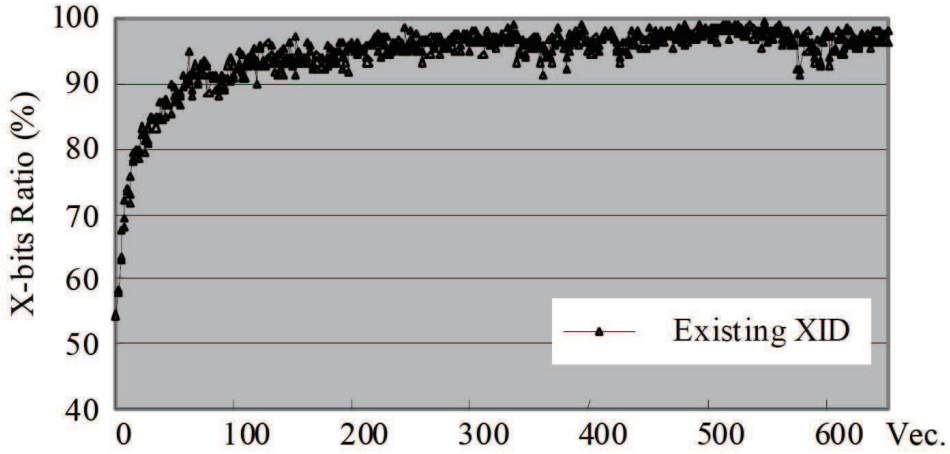


Figure 1.1: X-bit-Distribution [9]

X-filling has enough *X*-bits to reduce total transition count in circuit, but there might still be high transition count region, because faults are located closely or sensitization paths propagate through the same region. Nevertheless, most test vector generator collect as many faults as possible greedily to achieve high vector compress rate. That is to say, most faults are detected in the beginning vectors, and cause low *X*-rate as shown in Figure 1.1. Distribution-Controlling X-Identification (DCXID)[9] controls the distribution of *X*-bits identified from a set of fully-specified test vectors to reduce IR-drop. The approaches mentioned above are also known as *X*-identification. DCXID efficiently controls the distribution of *X*-bits to balance the distribution of *X*-bits in every test vector. However, the physical location of transition gates are not considered. In other words, many faults propagating through the same region may lead to IR-drop, no matter how *X*-rate is distributed evenly in the test vector.

In this paper, we propose a sophisticated care-bit-identification algorithm which identifies

IR-drop and peak current hot zones induced by high switching faults. Then, we remove these faults from the test vectors. To be clear, here we stress that IR-drop and peak current are not exactly the same thing. IR-drop increases gate delay and affects signal propagation. When VDD drops behind certain threshold, the result of testing will definitely be incorrect and leads to a negative false diagnosis. However, high peak current only increases the possibility of making incorrect diagnosis. Therefore, we not only focus on improving IR-drop but also reduce the peak current while removing faults.

Instead of blindly controls the average ratio of X-bits in each test vector, we carefully characterize the care bits of faults. Moreover, high transition count region may be caused by a group of essential faults. Therefore, the only solution to reduce switching activities without sacrificing fault coverage is to allow other test vectors to cover these essential faults.

In our work, we apply our algorithm after performing the physical location aware X-filling algorithm proposed in [6]. The *X*-filling of [6] fails to reduce transition count of certain regions if there are not enough X bits associated to these regions. Therefore, an iteration flow is designed to free a reasonable number of specified bits of test vectors to increase feasibility of X-filling and further reduce the switching activities.

The rest of this paper is organized as follows. In Section II we briefly introduce related works and background. In Section III, we describe our preliminaries. Section IV presents our proposed physical-location-aware algorithm to reduce IR-drop and peak current. Section V shows our experimental results, then we concludes this paper in Section VI.

Chapter 2

At-speed Testing Model

Before describing the motivation of our work, at-speed testing model is introduced first. In our work, we adopt the *launch-off-capture* scheme for at-speed scan-based delay test. Figure 2.1 shows an example waveform.

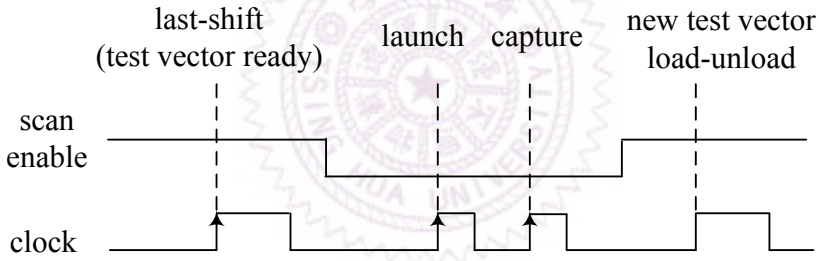


Figure 2.1: The waveform of launch-off-capture scheme.

In this approach, after the test vector is loaded into the scan chain (at *last-shift* pulse), two clock pulses are applied in capture mode. The first pulse *launches* the transition at target terminal, which is always the flip-flop output, and the second pulse *captures* the response from the flip-flop input at a scan cell. It can be regarded as two timing frames. The input vector of the first timing frame comes from the primary input and scan flip-flops. Then, the output vector of the first timing frame becomes the input vector of the second timing frame

as shown in Figure 2.2.

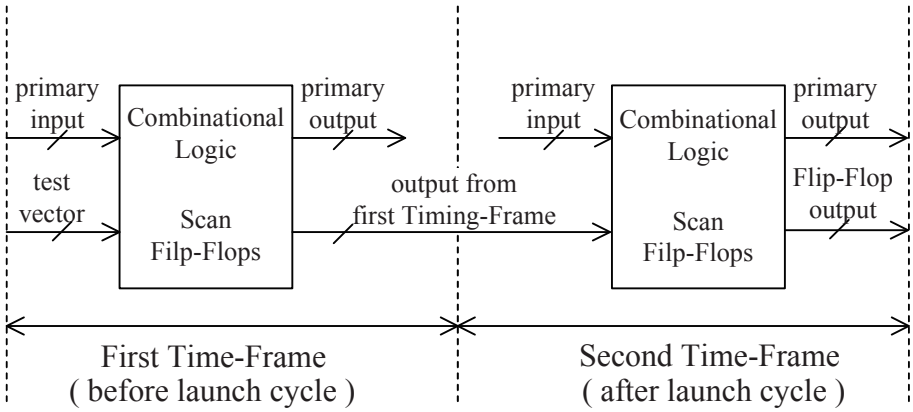


Figure 2.2: The timing frame form of launch-off-capture scheme.

Since the false delay path occurs between the launch pulse and the capture pulse, our goal is to minimize the impact of IR-drop effect during this test cycle. In other words, our goal is to minimize the switching activity of gates between the last-shift cycle (before launch cycle) and the launch cycle.

Chapter 3

Motivation

The *X*-ratio of test cubes are often high and the values set on unspecified bits affect the switching activity of an entire chip significantly. Therefore, many researches [6, 8, 11, 12] propose *X-filling* to reduce IR-drop. Here, *X-filling* is to fill *X*-bits of test vectors with suitable logic values (1 or 0) according to design constraint. Among others, Hsieh et al.[6] proposes *X-filling* approach to reduce switching activity by taking physical location into consideration. This *X-filling* approach can effectively reduce the switching activity in hot area, because it considers the physical location with high switching activities. However, the performance of the *X-filling* is limited by the characteristic of the *X*-bits. Take benchmarks b17 and b22 released from ITC'99 as an example. Table 3.1 and 3.2 show the ratio of the specified logic value in one hot target region. AL and BL represent the ratio of signals whose value are specified *after launch cycle* and *before launch cycle*, respectively. By Hsieh's *X-filling*, the switching activity of benchmark b17 in hot region can be decreased while that of benchmark b22 cannot be improved. From Table 3.1 and 3.2, we find that the ratio of specified value in hot region of benchmark b22 is more than that of b17 in AL. Due to the

Table 3.1: The Specified Value Ratio of Sereve IR-drop Region in b17

Pattern ID	BL(%)	AL(%)
109	85	77
195	77	65
18	80	70
183	65	61
514	71	79
90	80	70
156	49	48
219	72	70
418	77	77
316	66	60

Table 3.2: The Specified Value Ratio of Sereve IR-drop Region in b22

Pattern ID	BL(%)	AL(%)
19	100	100
137	93	100
37	100	100
136	100	100
41	97	100
51	100	100
240	100	100
9	100	100
4	100	100
157	59	100

lack of enough *X*-bits to perform *X*-filling, Hiesh's *X*-filling has little improvement on b22.

Moreover, according to our observation in benchmark b17, shown in Table 3.3. The columns labeled *X-ratio*, *AL-X-ratio*, *TC* and *#Gate* represent the *X*-ratio in initial test vector, the *X*-ratio in highest transition count region, the number of transition count and gates in highest transition region, respectively. Although the *X*-ratio in *vector447* and *vector449* are almost the same, the *X*-bit distribution in their highest transition count region are different. In other words, average the *X*-ratio in test vectors, may not result in average

Table 3.3: Initial Test Pattern Profiling in b17

pattern	X-ratio	AL-X-ratio	WSA	TC	#Gate
447	87.4%	36%	3.56	99	265
449	87.5%	26%	3.62	111	265

§ *WSA* is defined in section 4.3.

transition count in every region.

By aforementioned statements, we further define a rule for test relaxation to reduce switching activities of the target regions with physical location information. The rule for test relaxation is as follows.

- **Identifying faults that affect the hot target region:**

  Identifying care bits of these faults that propagates to a target region and relaxing care bit to *X*-bit give *X-filling* more control on switching activity in this region. The values of sensitization path passing through a hot target region are controlled by care bit.

With analyzing each fault with switching activities in terms of physical location, we can establish the test relaxation with physical location to reduce IR-drop.

Chapter 4

The Proposed Algorithm

While [9] distributes the ratio of *X*-bits evenly in test cube, we focus on test relaxation in test cube to reduce peak current and IR-drop in hot zone. We propose a physical-location-aware *X*-identification reduce both IR-drop and peak current in CUT using transition delay fault model in LOC (Launch-Off-Capture) mode described as follow.

4.1 The Power Grid Architecture

In our environment, power/ground distribution network shown in Figure 4.1 in [7] is adopted. The power rings are placed around the core chip. Four VDD and VSS pads are inserted to the respective rings. An adequate stripe number are inserted to connect power/ground ring according to circuit size. Then the rails draw power/ground from the nearby power stripe. By using stripes and rails, the standard cells are routed to power source.

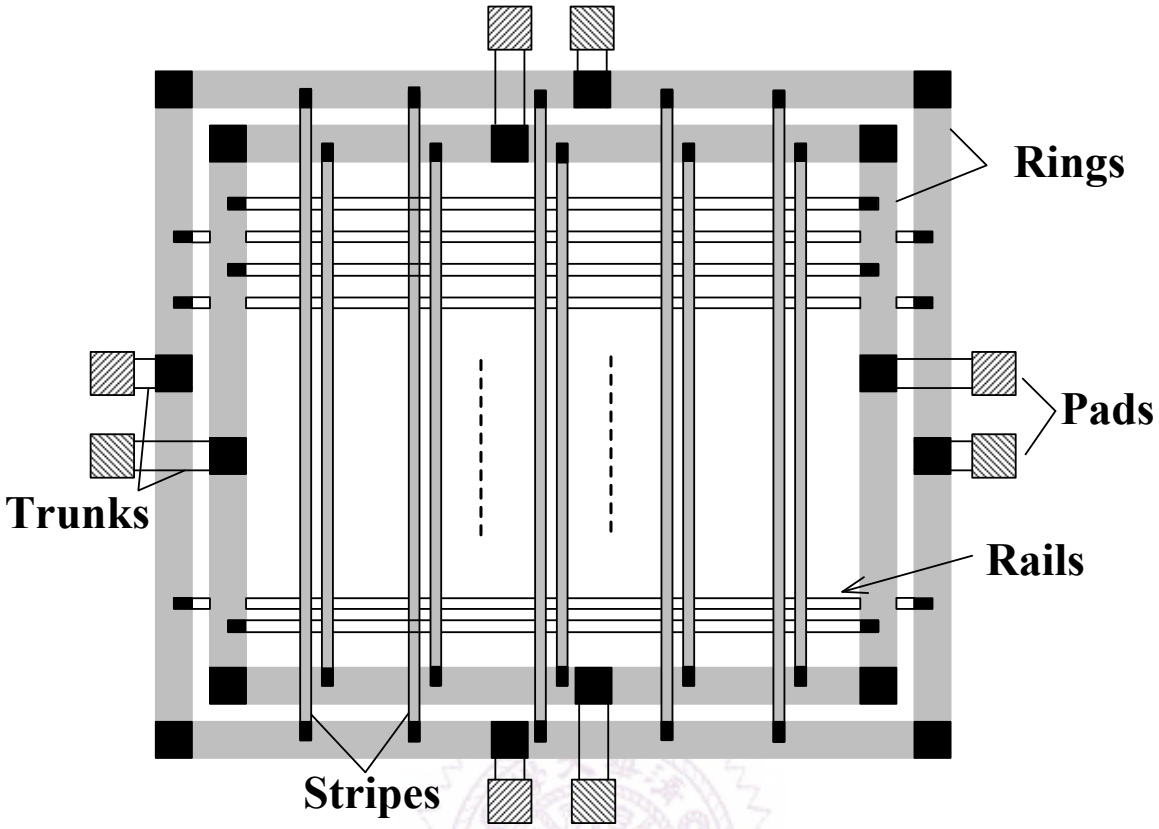


Figure 4.1: The power/ground distribution network

4.2 Overview of Our Proposed Method

In order to take physical location into account, our algorithm is performed after physical synthesis. An initial test cube (with *X*-bits) and a *X*-filled test cube (full specified) are also input to our algorithm. The objective of our algorithm is to identify more *X*-bits in the initial pattern for *X*-filling which result in high transition count after *X*-filling. Figure 4.2 is the overview of our algorithm. After placement and routing, physical information of the circuit is collected to be utilized in the following steps. First, *region_partition* is performed. Since the power grid structure is applied in our work, we divide the chip into several regions based on physical layout. All components in the chip are assigned to appropriate regions

according to their coordinate. For the characteristic of the power grid architecture described above, each region is surrounded by stripes and limited rails. If large number of cells switch simultaneously within the same region, the IR-drop effect in this region may increase the propagation delay. Then, our objective is to decrease switching activities in IR-drop hot region.

The next step is *target_vector_and_region_selection*. With a set of given critical paths and X-filled test cubes, the region switching activities in each test vectors is first calculated. The possible IR-drop vector is selected as *target vector* which leads the circuit to high LTC. Hence, the high transition count region is regarded as our *target region*. Then, the *candidate faults* which are either in the *target region* or propagating through the *target region* are selected because these faults lead the components in the *target region* to switch. With these physical location aware candidate faults, we perform a two phase *faults_removal* scheme to reduce excessive switching activities in the *target region*. After removing the candidate fault, there may remain unused care bits explained in section 4.6.3. Hence, we need to do *reclaim_of_unused_care_bits* every time when we finish *faults_removal*. Finally, we collect the dropped faults when removing faults and generate tolerance test vectors for them. The detail of *target_region_selection*, *candidate_faults_selection*, two phase *faults_removal* steps and *reclaim_of_unused_care_bits* are described in the following sections.

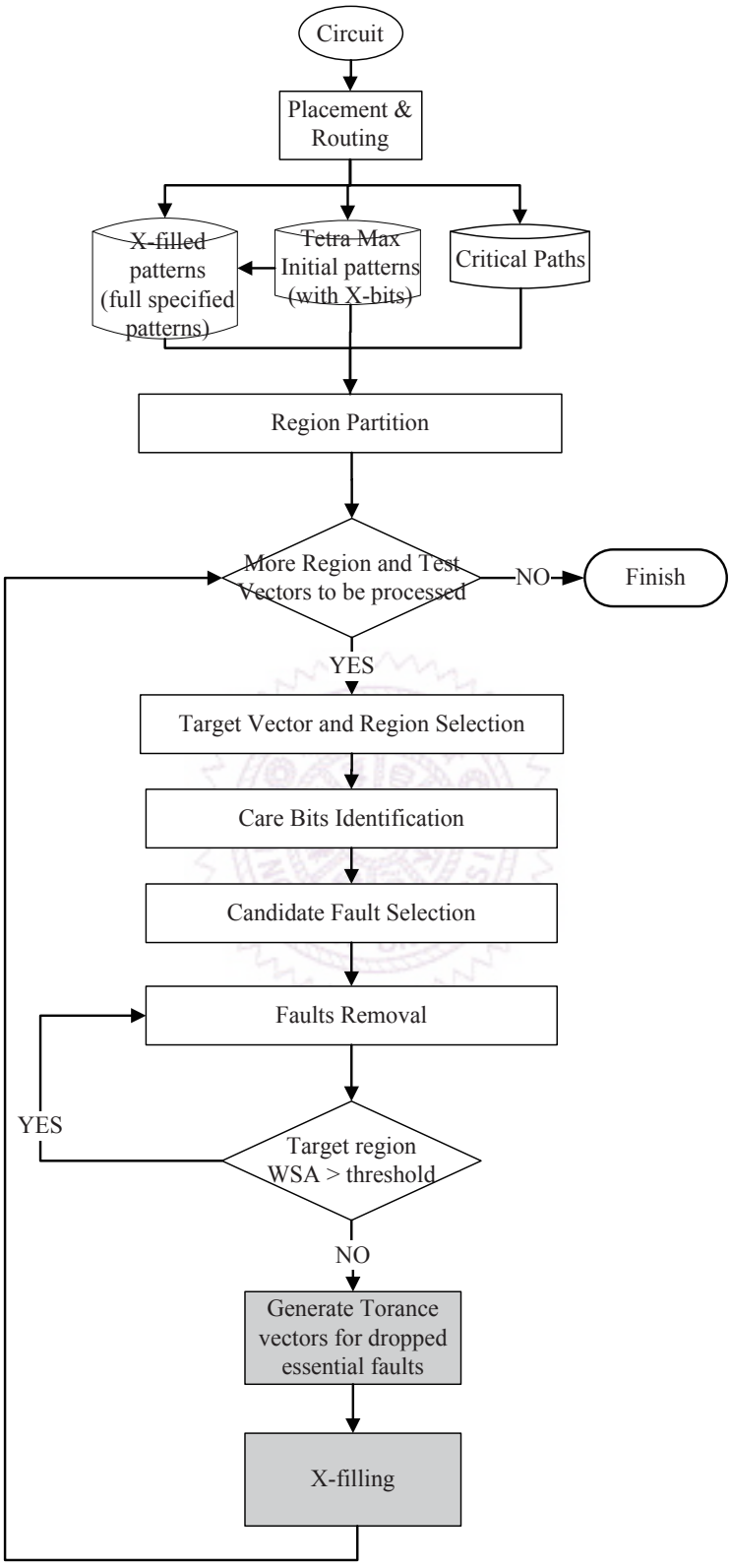


Figure 4.2: Physical-location-aware X-identification flow

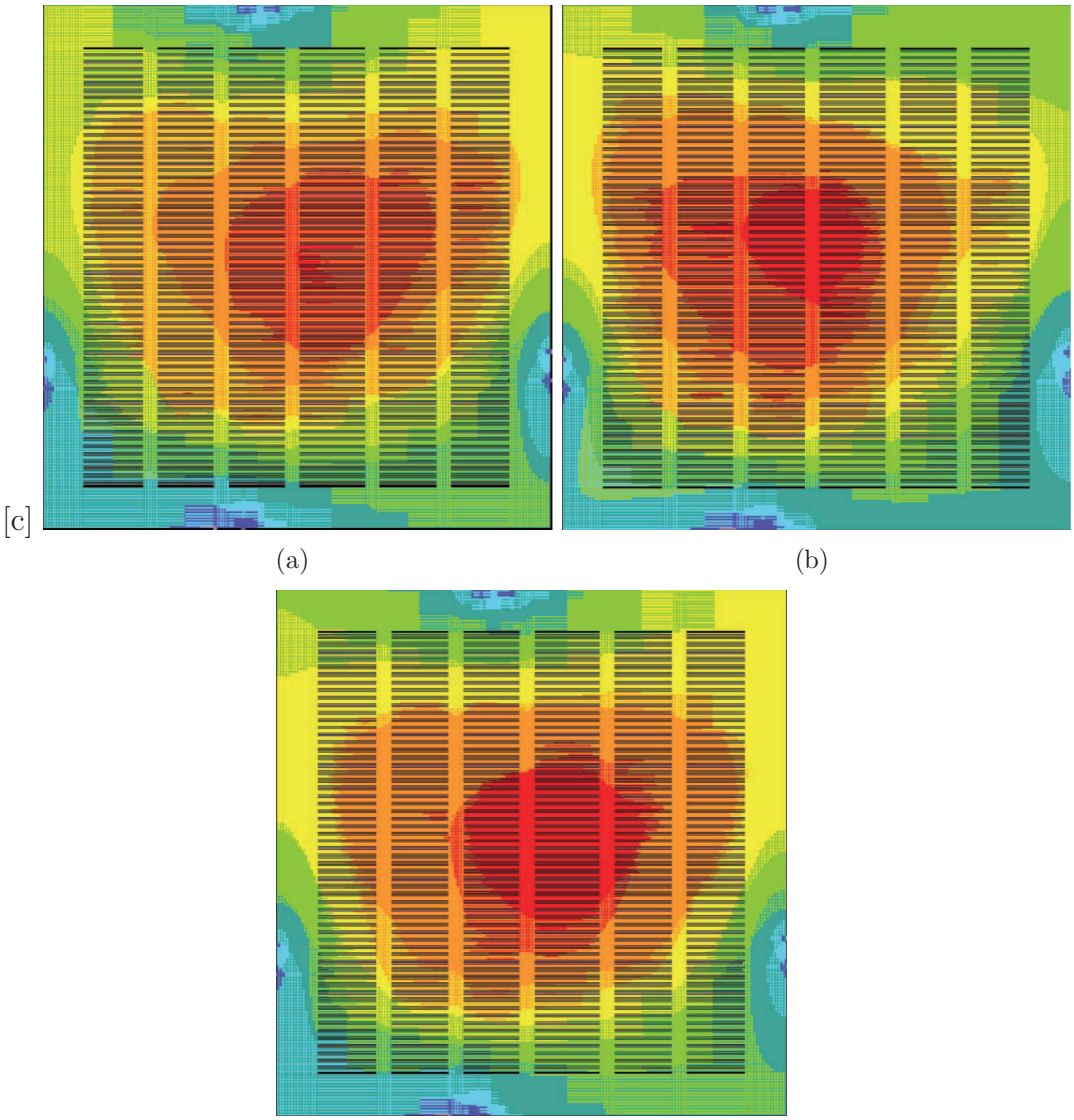
Table 4.1: Pattern comparison for test bench b22

pattern	grid cost	circuit cost
178	5.4542(NO.1)	260.383(NO.63)
37	3.8804(NO.245)	320(NO.3)
19	5.2188(NO.11)	325.318(NO.13)

4.3 Target Vector and Region Selection

This step is to recognize possibly IR-drop test vectors and regions. When we want to predict whether a test vector results in IR-drop or not, it is necessary to know whether total transition count or local transition count affects IR-drop most. Hence, we analyze Hiesh's *X*-filled test vectors of benchmark b22 with RedHawk because of their limited performance. We choose three vectors from b22 according to their properties - LTC and GTC. In Table 4.1, grid rank and circuit rank is sorted by LTC and GTC, respectively. We analyze these test vectors with RedHawk shown in Figure 4.3. We compare Figure 4.3(a) with Figure 4.3(b), by their GTC and LTC properties. It is showed that high LTC affect the region to IR-drop more than GTC. Thus, we select the patterns which result in high LTC but not GTC as our target vector and focus on highest LTC region to do our algorithm.

In order to discriminate IR-drop hot zone from the other region in test vectors, we propose a cost function - *weighted switching activities* (WSA) representing the supply current demand and the power consumption. Then, we set 90% of highest WSA_{region} within all of the test cube as our threshold, and process all of the vectors which has region over the threshold to reduce switching activities in these region. Our cost function, WSA_{region} is defined to



[c]

(a) (b)

(c)

Figure 4.3: IR drop analysis

represent the IR-drop impact of each region caused by the test vectors. For a region i, its $WSA_{region\ i}$ is defined as follow

$$WSA_{region\ i} = \sum_{gatej}^{\forall gate\ j \epsilon\ region\ i} ((1 + \alpha \cdot Cri_j) \times switching\ weight(type_j) \times \sum_{k\ \epsilon\ fanout\ of\ j} capacitance_k) \quad (1)$$

Table 4.2: Toggle type of gates.

toggle type	weight
$1 \leftrightarrow 0$	2
$1 \leftrightarrow X,\ 0 \leftrightarrow X$	0.25
$X \leftrightarrow X$	0.125
$0 \leftrightarrow 0, 1 \leftrightarrow 1$	0

where Cri_i represents whether if *gate i* is on critical path and defined as

$$Cri_i = \begin{cases} 1, & \text{if } gate\ i \text{ is on critical paths.} \\ 0, & \text{otherwise.} \end{cases}$$

where α is the weight used to emphasize the importance of *gate i* if *gate i* is on the critical path. Since gates on critical paths switching simultaneously would cause severe voltage drop and lead to delay defects, the region with more critical paths will be voltage drop hot zone.

In our algorithm, we follow Hsieh's $WSA_{region\ i}$ definition [6] and set α to 0.5 to balance the importance of IR-drop and criticality. $Type_j$ in equation (4.3) represents the type of the toggle $gate_j$. We define number of switching weight to represent each toggle type, showed in table 4.2. *Switching weight* represents the preference and flexibility to assign a specific transition. The higher the value, the less the preference (flexibility) is. Then we collect the test vectors which has $WSA_{region\ i}$ excess the threshold, and process X-identification direct to the region in excess of the threshold.

4.4 Care Bits Identification

After selecting the target vector to reduce switching activities, we identify the target faults with their care bits. Care bits which either control the value or propagate value of

faults to be observe. Without implementing fault simulation, we use TetraMAX to run fault simulation. For all specified scan cells in initial target vector, we set each of them to X one by one, and run fault simulation to know which faults are covered. Moreover, we only process few test vectors, the processing time on fault simulation would not be too long.

4.5 Candidate Target Faults Selection

For a target vector and target region, a number of faults are covered by running this vector. Among them, we select some candidate faults which are either in target region or propagated through the target region. Take Figure 4.4 as an example, the grey and white nodes represent target faults and gates, respectively. These three faults which either in the target region or propagated through the region would be regarded as our candidate faults. Removing faults from the coverage of this test vector will allow more X-bits in the initial vector. For a fault covered by a vector, we define its tf_{gain}:

$$tf_{gain} = WSA \times detectable\_vector\_\#$$

where WSA is the WSA in the target region and *detectable_vector_#* is the number of vectors covering this target fault. The more test vectors cover this fault, the less influence affect this fault removal in other test vectors. A large value tf_{gain} denotes that either this target fault result in large switching activities in target region or less influence after fault removal. We sort these candidates by tf_{gain} and remove fault begin with max tf_{gain}.

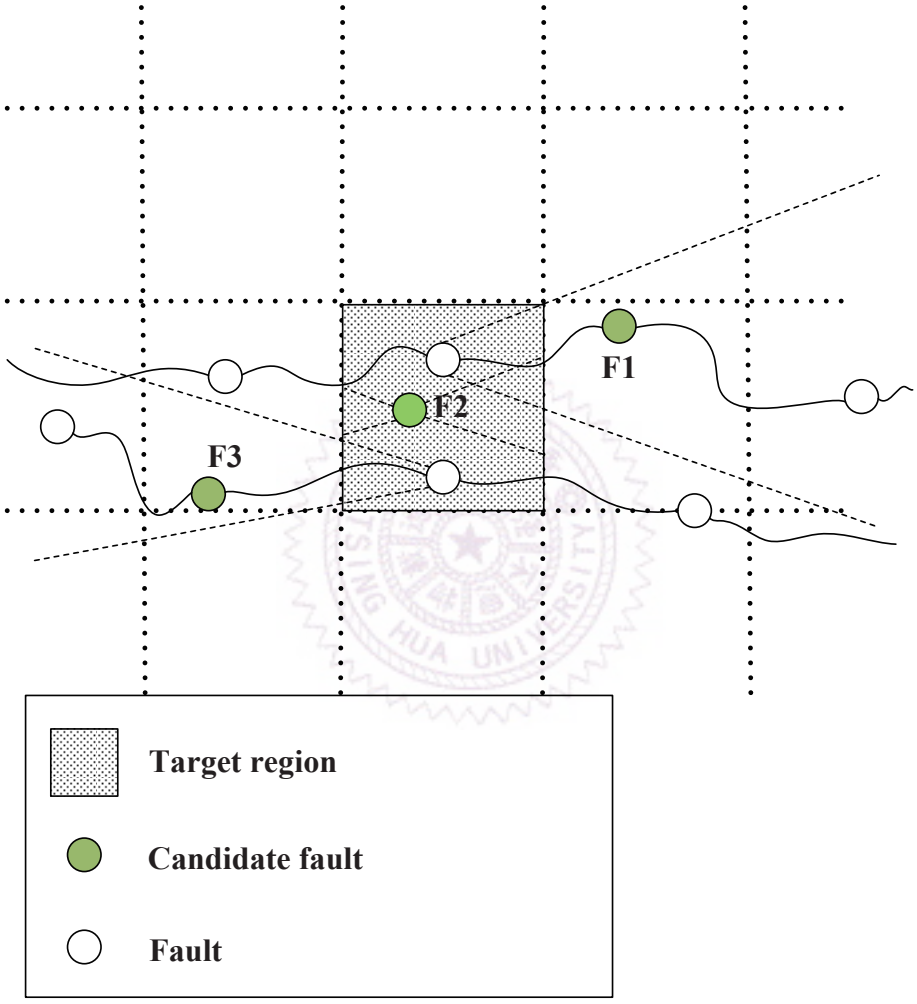


Figure 4.4: Fault propagation path

4.6 Faults Removal

To consider the fault coverage issue, we classify faults into non-essential and essential fault. Here, *essential fault* is defined as the fault covered by only one test vector. Otherwise, it is *non-essential fault*. It is well known that the transition fault model is path based delay model. That is to say, we cannot remove one target faults from the test vector without drop the other faults which are on the same propagation path. Taking Figure 4.5 as an example. There are two paths propagating through the target region with an essential fault on each of them. The grey and white node represent essential and non-essential fault, respectively. However, we can not reduce switching activities without fault coverage drop because there is an essential fault on each of them. Furthermore, Table 4.3 shows the ratio of essential care bits (the care bit in test vector detecting essential fault) to total sensitized care bits is over 50%. It means that essential faults distribution may limit the performance of XID, if they do not remove essential faults. For above observation, it is necessary to design an approach to remove essential faults to reduce switching activities with minimal overhead - generating new test vectors (tolerance vectors). Figure 4.6 shows the fault removal flow.

4.6.1 Non-essential Faults Removal

In this phase, we will try to remove non-essential faults to reduce transition count of the target region without penalty (generate tolerance vectors). According to tf_{gain}, the fault detected most will be the first choice to remove. When non-essential faults are targeted in

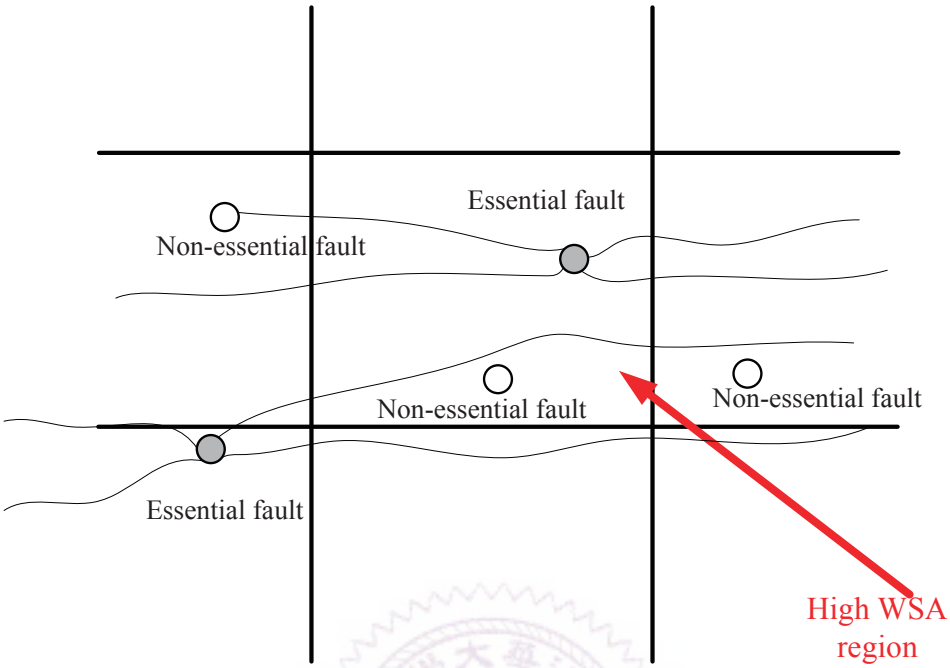


Figure 4.5: IR-drop with Essential Fault

Table 4.3: The Essential Care Bit Ratio of Top 10 Switching Activity Pattern in b22

pattern ID	Essential CB#	Tot. CB#	Ratio(%)
19	411	508	81
137	281	356	79
37	329	446	74
136	337	387	87
41	334	425	79
51	373	423	88
240	289	350	83
9	322	475	68
4	303	464	65
157	275	337	82

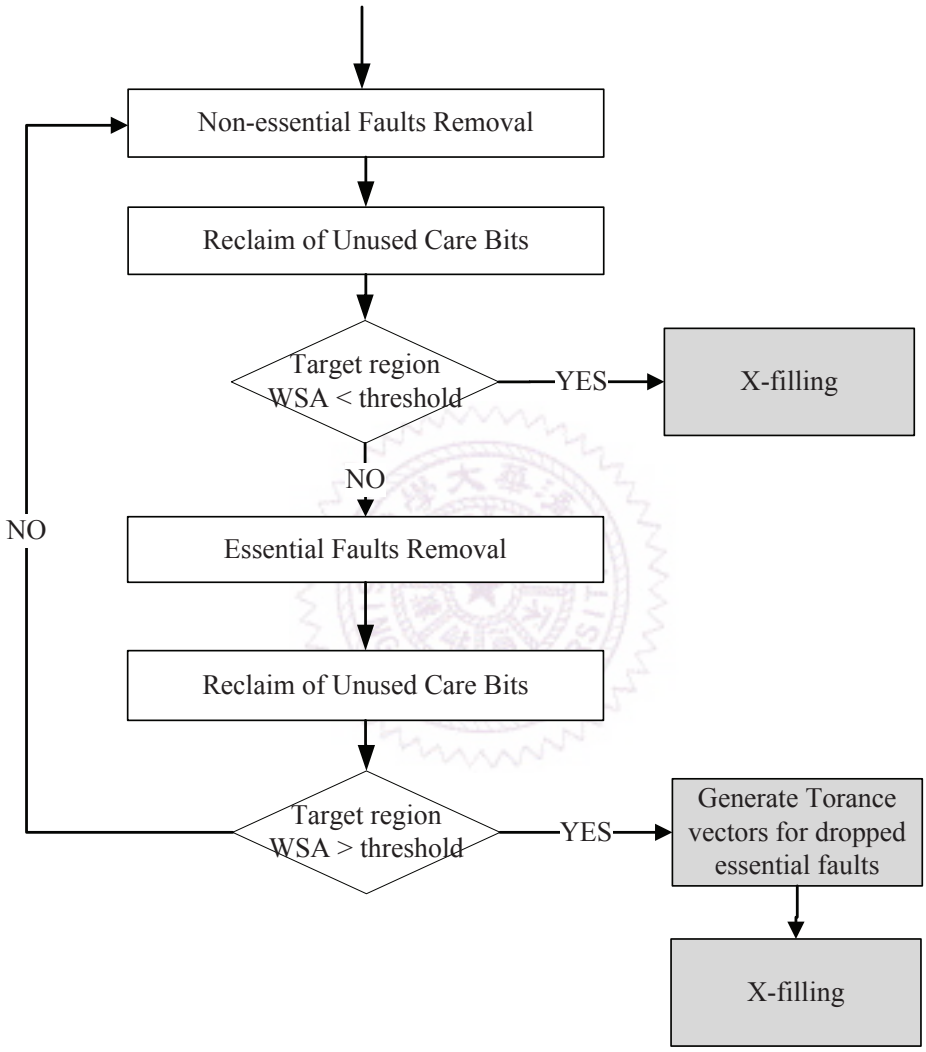


Figure 4.6: Flow of Faults Removal

earlier test vector, more faults are targeted than in later test vectors. Because most of the later test vectors are generated to target hard detected faults which will also toggle the faults on the same path which are covered in the earlier test vectors. That is the reason why the earlier test vectors result in peak current or IR-drop easily. However, these non-essential faults could be removed if they would not affect the other essential faults. For the purpose to keep fault coverage, we lock the care bits of the essential faults before we remove the non-essential faults.

4.6.2 Essential Faults Removal

In this phase, we remove a care bits of the candidate faults selected above to reduce switching activities of the target region. When the flow goes to this phase, there are no removable non-essential faults to reduce the switching activates of the target region. That is to say, the candidate faults may be either essential faults or on the propagation path of the essential faults. In order to take both cost in target region and the number of sensitizing essential fault into account. We model another gain function to estimate the gain of the each candidate care bits, then remove the care bit with highest gain. To be clear, candidate care bits is the controlling bits of these candidate faults. Because removing the observability bits can only stop the fault propagating to scan cell but not stop the transition of the fault. The gain of the care bits s defined as follow:

$$cb_{gain} = \frac{WSA\ in\ target\ region}{sensitize\ essential\ fault\ \#}$$

Then, we choose only one candidate care bit with maximum gain to remove and collect dropped faults to generate tolerance vectors. Notice that, every time when we remove a care bit in second phase without fixing target region, we go back to first phase to try painless solution first.

4.6.3 Reclaim Unused Care Bits

After identifying one care bit to X, we should reclaim the other unused care bits. As showed in figure 4.7, FF_2, FF_3, FF_4 only used to sensitize faults - G_1, G_4, G_5, G_7. When we remove faults G_1, G_4, G_5, G_7 by identifying FF_2 to X, FF_3, FF_4 will be redundant. They should be identified to X to extend the solution space of X-filling. Thus, we reclaim unused care bits right after X-identification. For this purpose, we mark the care bits of the remaining faults, then we set unmarked care bits to X to reclaim unused care bits.

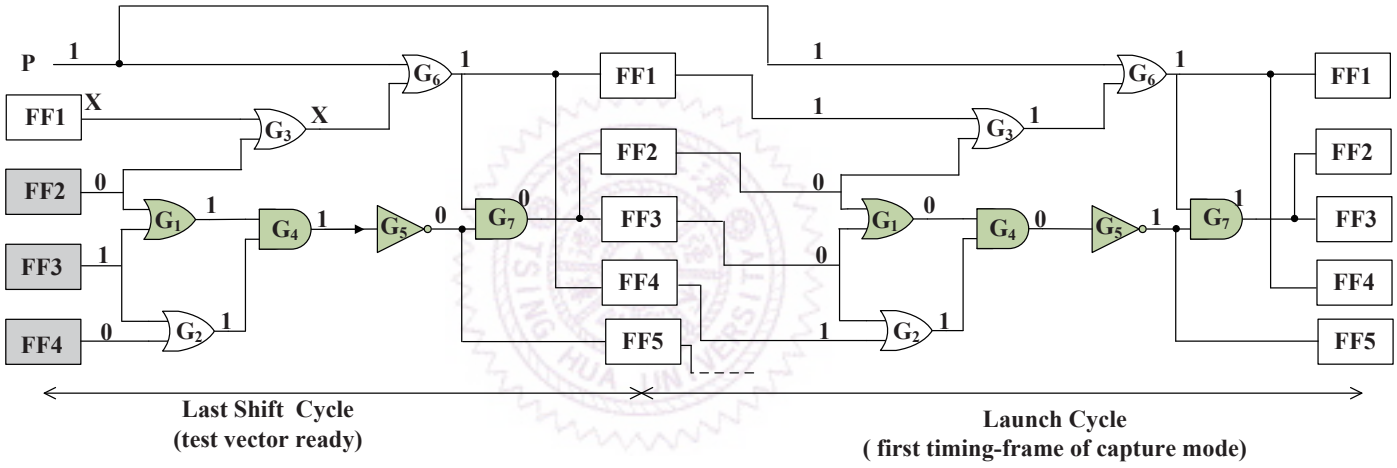


Figure 4.7: Reclaim care bits

Chapter 5

Experimental Results

We implemented the proposed method using C++ programming language and performed experiments on ITC'99 benchmark [10]. Figure 5.1 presents our experimental flow.

The circuits are described in VHDL and synthesized by Synopsys Design Compiler with TSMC 90nm cell library. Six kinds of gates including *BUFFER*, *INVERTER*, *NAND*, *NOR*, *AND* and *OR* are used for synthesis. The gate-level netlist and the test protocol in STIL format are generated. The input to SoC Encounter (SOCE) is the netlist and the output is a layout design with detailed physical location and the timing information after floorplaning, placement, and routing. Then the netlist and the test protocol are fed into TetraMax to generate test patterns with unspecified bits. Meanwhile, the timing information is used as input file for PrimeTime to produce critical paths information. Our algorithm takes the netlist of layout design (*.def), the test vector with unspecified bits, the test vector after *X*-filling and the critical paths information as input files, identifies some care bits, and relax them as *X*-bits to provide more space for *X*-filling.

Table 5.1 shows the information of benchmark circuits. The columns labeled *#PI*, *#FF*,

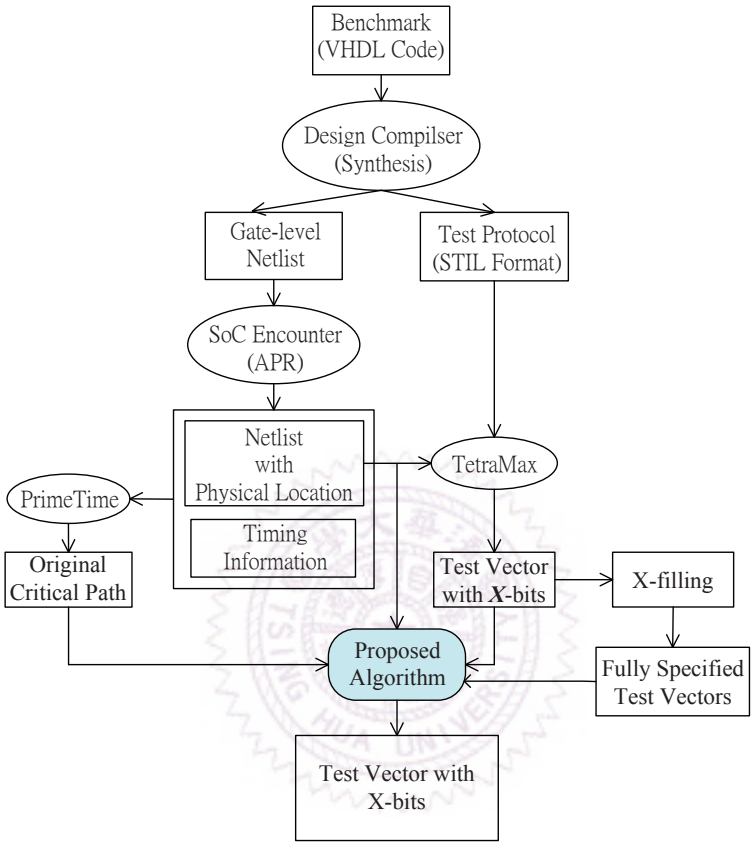


Figure 5.1: The overall flow of the experiment

and *#Gate* represent the number of primary input, the number of scan-chain flip-flop and the total number of gate count, respectively. The number of vertical stripes and the number of rows used to divide a layout into regions are listed in columns 5 and 6.

Table 5.1: Descriptions of circuits

Circuit	#PI	#FF	#Gate	#Stripe	#Row
b11	11	31	824	3	16
b12	9	121	935	3	16
b14	36	215	20328	3	99
b15	40	417	10289	3	115
b17	42	1317	30537	5	150
b20	36	430	25089	5	293
b21	36	430	25619	5	293
b22	36	613	38701	5	293

Test vectors are generated using TetraMax to achieve coverage grater than 80%, or the number of the test vectors larger than 700. To restrict the number of test vectors is due to long running time of RedHwak to process vector-based IR-drop simulation. Table 5.2 shows the information of generated test cube. The column labeled *#Vec* and *Fault Coverage (%)* represent the number of test vectors and the fault coverage by running these test patterns.

Table 5.2: Descriptions of the test cube

Circuit	#Vec	Fault (%) Coverage
b11	186	63.17
b12	278	80.38
b14	574	90.02
b15	653	71.38
b17	672	70.47
b20	575	85.48
b21	578	83.22
b22	576	86.02

We compare the results of local WSA before and after test relaxation. Local WSA is computed by the WSA summation of the components in the target region. Table 5.3 shows

Table 5.3: Comparison of Local WSA

	Average			Peak		Fault Coverage(%)		
circuit	orig. cost	our. cost	Imp.(%)	orig. cost	our cost	orig.	fixed	† D.F.#
b11	0.39	0.22	42.45	0.41	0.31	62.02	61.91	5
b12	0.28	0.03	90.84	0.28	0.03	80.14	79.99	8
b14	5.38	4.83	10.24	5.66	5.07	88.15	88.14	12
b15	2.72	2.57	5.68	2.87	2.85	71.10	71.05	13
b17	3.72	0.57	84.76	3.88	0.57	70.34	70.25	171
b20	4.53	3.89	14.12	4.98	4.30	85.36	85.36	1
b21	7.01	5.98	14.62	7.71	5.98	83.09	83.09	0
b22	5.12	4.54	11.32	5.45	4.87	85.86	85.85	19
Avg			34.25					

† D.F# is represented as dropped fault number

the result of our average WSA, peak WSA and dropped essential fault number. The results before applying test relaxation is our baseline and the columns labeled *(%)* are the reduction ratio as compared to the result after test relaxation.

From this table, we can find that our approach has significantly reduction on local WSA at the cost of dropping small number of essential faults. The improvement ratio of our Physical-Location-Aware X-Identification can achieve 34.25% in the average.

Table 5.4 shows the result of local transition count. Similarly, we compare the results before and after test relaxation. We can see the result of transition count is consistent with that of WSA. Hence, it can be said that our WSA cost function estimates the real switching activities and can be used to reduce the switching activities of the target regions.

Table 5.5 shows the result of global WSA. Global WSA is computed by means of the WSA summation of all components in the circuit. Obviously, our approach has little effect on

Table 5.4: Comparison of Local Transition Count

	Average			Peak	
circuit	orig. transition#	our transition#	Imp.(%)	orig. transition#	our transition#
b11	22	12	45.45	25	19
b12	18	0	100.00	22	1
b14	110	93	15.45	128	107
b15	59	39	33.90	66	44
b17	124	3	97.58	129	9
b20	86	67	22.09	93	71
b21	158	141	10.76	158	141
b22	110	92	16.36	124	110
Avg			42.70		

Table 5.5: Comparison of Global WSA

	Average			Peak	
circuit	orig. cost	our cost	Imp.(%)	orig. cost	our cost
b11	2.31	2.10	9.03	2.46	2.37
b12	1.27	1.25	1.88	1.46	1.46
b14	228.52	227.07	0.63	247.70	244.94
b15	36.60	33.99	7.14	39.01	37.69
b17	63.22	56.19	11.12	66.36	65.12
b20	185.08	184.83	0.14	196.99	196.99
b21	218.41	217.96	0.21	231.99	231.99
b22	307.09	305.35	0.56	325.32	323.21
Avg			3.84		

total transition count. Because the end condition of our algorithm is to satisfy the threshold of local WSA but not global WSA in circuit. That is to say, we can remove faults precisely which is led the target region to toggle without redundant fault coverage drop.

Chapter 6

Conclusion

In this paper, we have proposed a care-bit-identification algorithm which takes into consideration in high switching faults IR-drop and peak current hot zones. We have applied our algorithm after performing the physical location aware X-filling algorithm proposed in [6]. Then, we relax faults from test vector that results in IR-drop. Therefore, our test relaxation give *X-filling* more control on switching activity in the high WSA region. The experimental results show that we have an average of 42.70% transition reduction improvement for the IR-drop in hot zone.

Bibliography

[1] Gatej, J., Lee Song, Pyron, C., Raina, R., "Evaluating ATE features in terms of test escape rates and other cost of test culprits", *Test Conference*, pp. 1040 - 1049, 2002

[2] B.Swanson and M.Lange, "At-speed testing made easy," EE times, 3, June 2004.

[3] L.-T. Wang, C.-W. Wu, and X. Wen, (Editors), VLSI Test Principles and Architectures: Design for Testability, San Francisco: Elsevier, 2006.

[4] P. Girard. "Survey of Low-Power Testing of VLSI Circuits." IEEE Design and Test of Computers, 19(3):80V90, May-June 2002.

[5] Q. Xu, D. Hu, and D. Xiang. "Pattern-Directed Circuit Virtual Partitioning for Test Power Reduction." Proc. International Test Conference (ITC), paper 25.2, 2007.

[6] Wen-Wen Hsieh, I-Sheng Lin and TingTing Hwang, "A Physical-Location-Aware X-filling Method for IR-Drop Reduction in At-Speed Scan Test", *The Design, Automation, and Test in Europe (DATE) conference*, 2009.

[7] N. Ahmed, M. Tehranipoor, V. Jayaram, "A novel framework for faster-than-at-speed delay test considering IR-drop effects," in Proceedings of the IEEE/ACM international Conference on Computer Aided Design, pp.198-203. November 2006.

[8] X. Wen, Kohei Miyase, Tatsuya Suzuki, Seiji Kajihara, Yuji Ohsumi and Kewal K. Saluja, "Critical-Path-Aware X-Filling for Effective IR-Drop Reduction in At-Speed Scan Testing," DAC 2007.

[9] Kohei Miyase , Kenji Noda, Hideaki Ito, Kazumi Hatayama, Takashi Aikyo, Yuta Yamato, Hiroshi Furukawa, Xiaoqing Wen, Seiji Kajihara. "Effective IR-drop reduction in at-speed scan testing using Distribution-Controlling X-Identification" International Conference on Computer Aided Design ,paper Pages 52-58 ,2008

[10] "http://www.cerc.utexas.edu/itc99-benchmarks/bench.html"

[11] X. Wen, K. Miyase, S. Kajihara, T. Suzuki, Y. Yamato, P. Girard, Y. Ohsumi, and L. T. Wang,"A Novel Scheme to Reduce Power Supply Noise for High-Quality At-Speed Scan Testing," Proc. Int'l Test Conf., Paper 25.1, 2007.

[12] Jia Li, Qiang Xu, Yu Hu, Xiaowei Li, "iFill: An Impact-Oriented X-Filling Method for Shift- and Capture-Power Reduction in At-Speed Scan-Based Testing", *The Design, Automation, and Test in Europe (DATE) conference*, 2008.